JEDEC STANDARD

PSO-N/PQFN Pinouts Standardized for 14-, 16-, 20-, and 24-Lead Logic Functions

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PSO-N/PQFN PINOUTS STANDARDIZED FOR 14-, 16-, 20-, AND 24-LEAD LOGIC FUNCTIONS

(From JEDEC Board Ballot JCB-05-151, formulated under the cognizance of the JC-40 Committee on Digital Logic)

1 Scope

This standard defines device pinouts for 14-, 16-, 20-, and 24-lead logic functions. This pinout standard specifically applies to the conversion of DIP-packaged logic devices to PSO-N/PQFN packages logic devices.

The purpose of this standard is to provide a pinout standard for 14-, 16-, 20-, and 24-lead logic devices offered in 14-, 16-, 20-, and 24-lead PSO-N/PQFN packages for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

2 Terms and definitions

For the purposes of this standard, the following apply:

DIP: Dual In-line Pin Package

HW-PQFP/HV-PQFP/PSO-N: Dual Compatible Thermally Enhanced Plastic Very Thin and Very Very Thin Fine Pitch Quad Flat No Lead Package (MO-241 Issue B, variations AA, BA (14-lead), AB, BB (16-lead), and AC, BC (20-lead))

HWF-PQFN/HVF-PQFN: Thermally Enhanced Plastic Very Thin and Very Very Thin Fine Pitch Quad Flat No Lead Package (MO-220 Issue J, variations VGGD-2 and VGGD-8 (24-lead))

3 Pinout standard

3.1 Description

The following criteria shall be used to convert existing 14-, 16-, 20-, and 24-lead logic devices offered in 14-, 16-, 20-, and 24-pin DIP packages to 14-, 16-, 20-, and 24-lead PSO-N/PQFN packages.

3 Pinout standard (cont'd)

3.2 14-lead PSO-N (MO-241, Variation AA, BA)

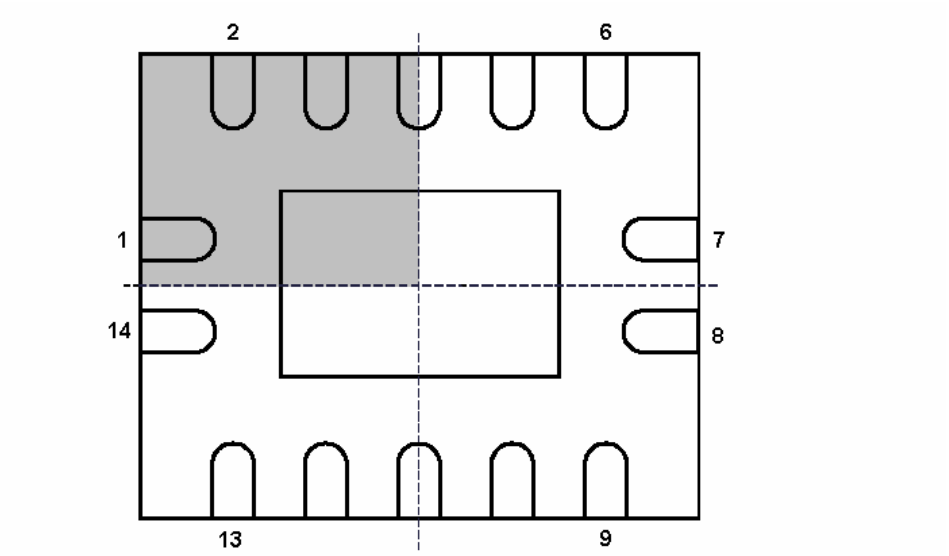

Figure 1 — Pin configuration for MO-241, variation AA, BA (bottom view)

3.2 Pin conversion from 14-pin DIP to 14-lead PSO-N

The pin conversion adopts the naming convention of the logic devices in the 14-pin DIP packages.

	Pin Number													
14-pin DIP	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**
14-lead PSO-N	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**

Figure 2 — 14-lead pin conversion table

3 Pinout standard (cont'd)

3.3 16-lead PSO-N (MO-241, Variation BA, BB)

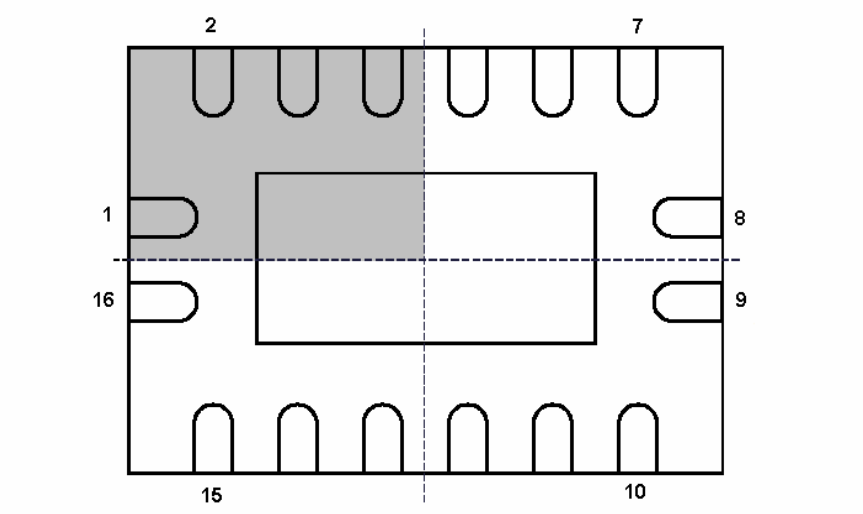

Figure 3 — Pin configuration for MO-241, variation BA, BB (bottom view)

3.4 Pin conversion from 16-pin DIP to 16-lead PSO-N

The pin conversion adopts the naming convention of the logic devices in the 16-pin DIP packages.

	Pin Number															
16-pin DIP	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**
16-lead PSO-N	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**

Figure 4 — 16-lead Pin Conversion Table

3 Pinout standard (cont'd)

3.5 20-lead PSO-N (MO-241, variation AC, BC)

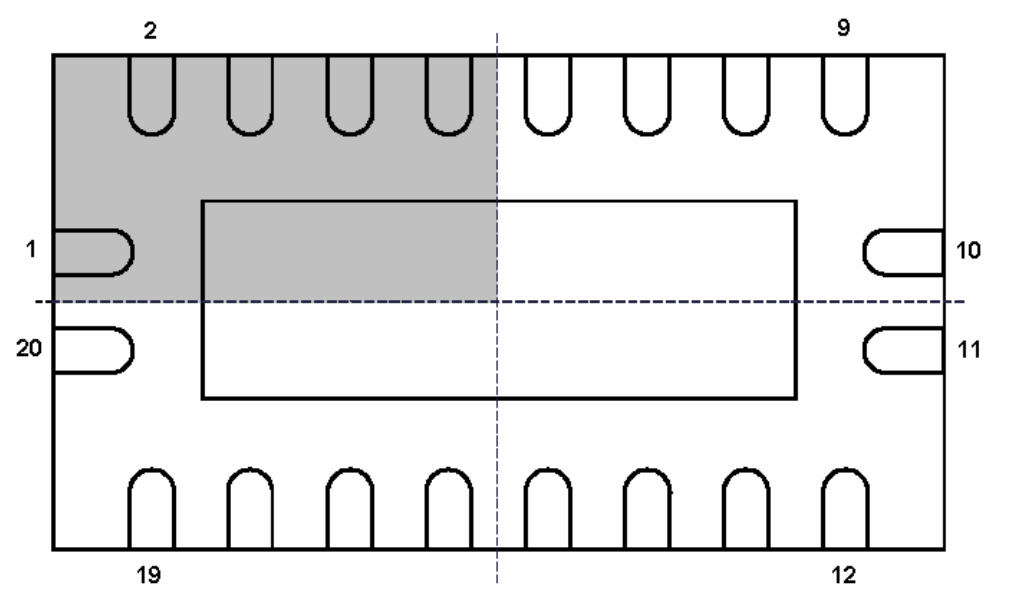

Figure 5 — Pin configuration for MO-241, variation AC, BC (bottom view)

3.6 Pin conversion from 20-pin DIP to 20-lead PSO-N

The pin conversion adopts the naming convention of the logic devices in the 20-pin DIP packages.

	Pin Numbers									
20-pin DIP	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**
20-lead PSO-N	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**
20-pin DIP	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**
20-lead PSO-N	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**

Figure 6 — 20-lead pin conversion table

3 Pinout standard (cont'd)

3.7 24-lead PQFN (MO-220, variations VGGD-2 AND VGGD-8)

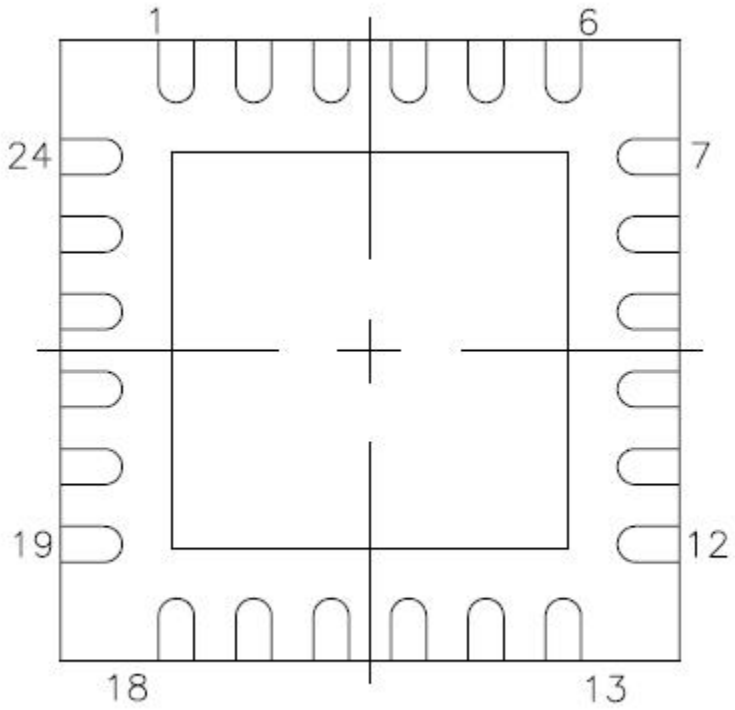

Figure 7 — Pin configuration for MO-220, variations VGGD-2 and VGGD-8, (bottom view)

3.8 Pin conversion from 24-pin DIP to 24-lead PQFN

The pin conversion adopts the naming convention of the logic devices in the 24-pin DIP packages.

	Pin Numbers											
24-pin DIP	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**
24-lead PQFN	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**
24-pin DIP	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**
24-lead PQFN	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**

Figure 8 — 24-lead Pin Conversion Table

4 Reference to other applicable JEDEC standards and publications

JEP95, *JEDEC Registered and Standard Outlines for Solid State and Related Product*

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